# INDIAN INSTITUTE OF TECHNOLOGY DHARWAD
## Off Pune Bengaluru Highway, Near High Court, Dharwad, Karnataka - 580011

## TENDER FOR SUPPLY AND INSTALLATION OF EQUIPMENT (REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES) AT INDIAN INSTITUTE OF TECHNOLOGY DHARWAD

## NOTICE INVITING TENDER (NIT) / RFP

| | |
|---|---|
| Tender No. | **IITDH/MMD/RnD/2021-22/026** |
| Description | **TENDER FOR SUPPLY & INSTALLATION OF EQUIPMENT (REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES) AT INDIAN INSTITUTE OF TECHNOLOGY DHARWAD** |
| Tender Date | 14.01.2022 |
| Tender Category | Goods |
| Tender Type | Open Tender |
| No. of Covers | 2 |

**Covers Information / Submission of Bids**

| Cover No. | Cover Type | Description |
|---|---|---|
| **1** | Technical | Schedule of Requirement and Compliances, Bidders Information, Previous Supply Orders etc. |
| **2** | Financial | Financial Bid |

**Two Bid System: -**
The two bid system will be followed for this tender. In this system bidder must submit their offer in separate sealed envelopes as – Technical Bid (Envelope No. A) and Commercial Bid (Envelope No. B).
Both these sealed covers are to be put in a bigger cover which should also be sealed and duly super-scribed with our Tender No. & Due Date and to be submitted to IIT Dharwad.
**Note:** The technical offer should not contain any price information. If the price quoted is submitted in technical bid the tender will be rejected by IIT Dharwad.
Initially Technical Bids will be opened and evaluated by the purchase committee. Commercial bids of only Technically qualified bidders will be opened later.
Contract/ Purchase Order will be awarded to the **lowest bidder (L-1) identified.**

| | |
|---|---|
| Form of Contract | Buy |
| Bid Validity (Days): | 90 Days |
| Period of Work/Delivery Period (Days) | 30 Days |
| Start date for Submission of queries via email to armm@iitdh.ac.in | 14.01.2022 |
| End date for Submission of queries via email to armm@iitdh.ac.in | 21.01.2022 till 11:00 AM |
| Date of rebuttal/reply of queries (to be uploaded on the website) and publishing revised tender (if required) | 21.01.2022 04:00 PM |
| Contract Type: | Open Tender |
| Delivery Location: | IIT Dharwad, Karnataka, India |
| Pin Code | 580011 |
| Bid Submission Start Date | 14.01.2022 |
| Bid Submission End Date & Time | 05.02.2022 till 10:00 AM |
| Place of Submission of Bid | The Assistant Registrar (MMD), IIT Dharwad<br>Off Pune Bengaluru Highway, Near High Court, Dharwad,<br>Karnataka- 580011, India |
| Bid Opening Date & Time | 05.02.2022 at 11:00 AM |
| Bid Opening Place | The Assistant Registrar (MMD), IIT Dharwad<br>Off Pune Bengaluru Highway, Near High Court, Dharwad,<br>Karnataka- 580011, India |
| Other Terms & Conditions | Warranty for five years from the date of installation and commissioning. |
| Tender Inviting Authority: | The Assistant Registrar (MMD), on behalf of Director, IIT Dharwad<br>Address: Off Pune Bengaluru Highway, Near High Court, Dharwad,<br>Karnataka- 580011, India |

Sd/-
Assistant Registrar (MMD), IIT Dharwad
(For and on behalf of Director, IIT Dharwad)

## Section - I: Invitation of the Bids & Submission Procedure details

1. Indian Institute of Technology Dharwad invites sealed tenders (under two bid system) from reputed suppliers/manufacturers OR authorized dealers for supply & installation of equipment (REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES.) as per the technical specifications given in the schedule annexed to the tender.
2. The bidder should note that the technical specifications mentioned in **Section IV** form the core of the product. The offers must strictly be as per the specifications given. At the same time, it must be kept in mind that mere copying of our specifications in the quotation shall not make the technical bid eligible for consideration. A bid has to be supported with original catalogue OR the schematic of the quoted item duly signed and the same must be sent along with the technical bid. Non-compliance with above shall be treated as incomplete/ambiguous and the bid may be ignored without giving an opportunity to the bidder for further clarification/negotiation etc.
3. In order to specify/modify technical specifications of the equipment and clarify various issues as may arise, a query session (by email) for clarification is provided. Resultant rebuttal/re-publishing of modified RFP (as the case may be) will be published, if required. **The bidders are advised to utilise the period given for clarifying any issue pertaining to RFP and to bring out any limitation / suggestion in the RFP. After the period is over, no issue will be addressed and the institute will assume general acceptance of RFP terms and conditions**. Prospective bidders have to submit their bids post rebuttal/modification in RFP (as the case maybe).
4. Any item not specifically mentioned in the tender document but essential in the opinion of the bidder for successful supply and installation of equipment (REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES), should be brought to the notice of the IIT Dharwad within the pre-bid clarification period and before end date of submission of queries. On clearance from our side, the same may be included in the modified RFP (as the case may be). However, the decision as to whether to consider such items or not, rests with the Institute.
5. The bidder shall ensure that the bid submitted by him includes all accessories (as per annexures) for full execution of contract. The bidder shall not charge extra for additional items required to meet the operational requirement at the stage of installation and commissioning.
6. Quantity requirements of each item as per the specification enclosed at **Section IV**.

| Sl. No. | Particulars of the item(s) | Requirement |
|---|---|---|
| (a) | SUPPLY & INSTALLATION OF EQUIPMENT (REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES) AT INDIAN INSTITUTE OF TECHNOLOGY DHARWAD | Individual item requirements as per **Section IV** |

7. **It may kindly be noted by all the prospective bidders that the tender will be awarded to the lowest successful bidder (L-1) for the price quoted in Sl.No.1 of Section V (as per tender subject).**

# Procedure for Bid submission

8. Every page, containing the said procedure for submission of bid and other important conditions, are to be signed by the bidder (to be serially numbered & bounded) and to be submitted along with their Technical bids towards their acknowledgement that they have gone through all the contents in these pages and in the Annexure as well and they are agreeing to comply to all of the conditions mentioned there. Non adherence to this may lead to the disqualification of the bid without further notice.

9. Two bid system: The offers/bids are to be submitted under a two bid system, namely (i) Technical Bid and (ii) Commercial Bid. The Technical Bid must contain all the details as specified in the Annexures along with the terms and conditions whereas Commercial Bid must indicate the quantity & rate only. There must not be any price element in the technical bid.

10. Sealing & marking of bid: The tender should be submitted in a proper manner with index for easy identification i.e.: -

| Envelope Number | To be super-scribed as |
|---|---|
| A | Technical Bid documents |
| B | Commercial Bid / Price Bid / BOQ |

**Envelope – A** (duly sealed): Should contain the documents as listed under Technical Bid Qualification.
**Envelope – B** (duly sealed): should contain the Commercial Bid (strictly as per the format provided).

Both the above envelopes should clearly be marked on top about the type of envelopes (i.e. A or B), details of contents in envelopes and name of agency submitting the bid.

The envelopes (A & B) after sealing must be kept in one bigger envelope and shall be addressed to:
The Assistant Registrar (MMD)
IIT Dharwad, Off Pune Bengaluru Highway,
Next to High Court, Dharwad - 580011, Karnataka, KA, INDIA

The bigger envelope must be sealed and must bear the following identification on top: -
Tender for 'SUPPLY & INSTALLATION OF EQUIPMENT (REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES.)'
a) Tender Number:_____Date: _____ and
b) Name and Address of the Bidder.
If the outer envelope is not sealed and not marked as above, the Institute will assume no responsibility for the misplacement or premature opening of Bid.

11. **Submission of tender**: The tender can be personally dropped in the tender box (kept near the IIT Dharwad building entrance outside MMD Section under supervision of a security guard) on all working days during working hours (except Saturday, Sunday & Holidays) before the date and time as specified in the Tender Notice and up to 10.00 AM on the last date of submission of tender. The tender can also be sent by registered post to The Assistant Registrar (MMD), Indian Institute of Technology Dharwad, Off Pune Bengaluru Highway, Next to High court, Dharwad - 580011, Karnataka, INDIA. Tender shall not be received after expiry of the time as specified in the tender notice. Late bids will not be accepted. However, in case the due date of tender submissions happens to be a holiday or office is closed due to any reason, then the tender submission date will automatically extend to the next working day (end submission time remains same).

12. **TECHNICAL BID DOCUMENTS & ELIGIBILITY CRITERIA:**

Only those bidders fulfilling the following Eligibility Criteria (supported by documents) are expected to participate in the Tender **(all criteria to be mandatorily fulfilled for technical qualification)**: -

| S. No. | Eligibility Criteria | Document required |
|---|---|---|
| a | Duly signed & stamped copy of the entire tender document. | The entire tender document to be duly signed & stamped by the bidder on each page. |
| b | PAN Card and GST certificate | Copy of PAN Card and GST certificate to be provided. |
| c | Income tax returns (ITRs) for last three consecutive financial years | Copy of Income tax returns for last three consecutive financial years (period from 2018-19, 2019-20 and 2020-21). |
| d | Proof of establishment of company/business for a period of more than 3 years. | The Bidder/OEM must be a reputed supplier/ manufacturer/ authorized dealer/authorized distributor/ authorized stockist/ channel partner in the business of supply and installation of REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES. for a period not less than 3 years (i.e. must be in this business from 2018 or earlier). The certificate of incorporation or any other relevant certificate to this effect is required to be enclosed.<br>The vendor must have supplied systems to Academic institutions which have been used in various electrical simulation projects<br>Vendor should provide details of their project team hierarchy with qualification and experience for in-house test facilities, infrastructure, and past experience in delivery of similar hardware<br>Vendor provided solution must be based on COTS hardware. It must be scalable and flexible allowing easy integration with new controllers.<br>**If necessary, the representative of IIT Dharwad may visit the Bidder/OEM Ex-Works for evaluation.** |
| e | Previous experience & copy of performance certificates along with Purchase Orders | Vendor should have experience in developing real-time HIL facilities for the Electrical Industries and preferably for Power System and power electronic applications.<br>The bidder/OEM must have successfully executed with IITs/ NITs/ IISc/ IISERs/ Central Universities/ laboratories of national importance.<br>Copy of at-least one performance certificate for supply and installation of real-time hardware-in-loop facilities (along with requisite purchase orders) to IITs/ NITs/ IISc/ IISERs/ Central/Govt. Universities/laboratories of national importance. |
| f | Declaration that the bidder / OEM had not been blacklisted or debarred anywhere in India or abroad by any organization. | A Certificate/Undertaking on the letter head of the Company to the effect that the bidder/ Manufacturer had not been blacklisted or debarred anywhere in India or abroad by any organization. |
| g | Bidder turnover for last 3 years should be minimum 5Cr. | Financial details should be submitted for the same. |
| g | **Duly filled and completed Section-IV**<br>• Compliance for commercial terms of tender<br>• Compliance for technical specifications of the equipment to be supplied<br>• Bidders information & Reasonability of prices | The following information on the letter head of the company / bidder:<br>• Compliance for commercial terms of tender<br>• Compliance for technical specifications of the equipment to be supplied<br>• Bidders information & Reasonability of prices |

13. The tenderer must submit all documents required for evaluation of technical bid and sought in the RFP as forming part of technical evaluation with signature and seal of the competent authority of the firm. In the event of non-receipt of any of the documents forming part of Technical Bid, tenderer may be disqualified from the process. No paper relating to the technical bid will be received during the Technical Bid evaluation or afterwards except for cases recommended & decided by the Procurement Committee. Further, any separate correspondence in the matter shall also not be entertained.

14. During evaluation of the Technical Bid, the Procurement Committee will scrutinize the documents mentioned above and may forward any or all the documents to the concerned authorities for verification and authentication. In case of any document(s) as submitted by the tenderer is found/reported to be fake, the tenderer will be out of the tendering process and suitable legal action may be initiated against the tenderer.

15. Besides, scrutinizing the documents submitted with the Technical Bid, the tenderer may be interviewed by the Committee to assess the eligibility, capability, and suitability of the tenderer. As such, the presence of the tenderer or any authorized representative of the tenderer in the Technical Bid meeting & commercial bid opening or as and when desired by authorities of IIT Dharwad is preferable.

16. The above mentioned basic eligibility conditions and additional clauses are broad guidelines for pre-qualification and the Director, IIT Dharwad hereby reserves the right to relax/ alter/ modify/ add any or all the conditions.

17. **Delivery terms (only D.D.P. IIT DHARWAD mode of delivery acceptable)**:

Items should be door delivered at IIT Dharwad, Karnataka, India – 580011.
**In case of indigenous supplies**, the bidder is requested to specify it clearly in Section-IV of this document. In order to obtain the concessional GST certificate, the bidder must quote in INR only and the delivery term acceptable shall only be door delivery at IIT Dharwad. The supplier should arrange for entire process from origin of equipment to the Stores at IIT Dharwad (including charges for safe packing, Marking & labeling, loading charges, road/air freight, insurance of goods, unloading charges, transport & unloading at buyer destination, installation, commissioning, demonstration and training; within the quoted price).

18. **Freight & Insurance**:

No freight and insurance charges will be provided and the materials are to be delivered at IIT Dharwad WALMI Campus, IIT Dharwad at the cost and risk of the supplier/Bidder within quoted price as per the delivery terms mentioned in the above paragraphs.

19. **Warranty declaration**:

a. The Bidder/supplier must give an unconditional warranty and comprehensive on-site support and maintenance for a period of **five years** from the date of successful installation and commissioning.
b. Any deviation in the equipment and the specification from the accepted terms and conditions may lead to rejection and non-acceptance of stores. In such case, the bidder/manufacturer is required to supply all the items in the specified form to the satisfaction/ specifications mentioned in the order and demonstrate at their own cost. The payments shall be made only after receiving the materials as per required specification and quality to the satisfaction of the competent authority of IIT Dharwad.

20. **Supply & Installation:**

a. The supplier is required to carry out the supply, & installation of the subject items at the IIT Dharwad installation site within the delivery period; otherwise the penalty clause will be the same as per the supply of material (refer to the liquidated damages below).

b. In case of any mishandling/damage to items and supplies during carriage from the origin of items to the installation site, the supplier has to replace it with new items/supplies immediately at his own risk of cost. Supplier will settle his claim with the insurance company as per his convenience. IIT Dharwad will not be liable for any type of losses in any form.

21. **Liquidated Damages:**

The equipment should be delivered/dispatched to destination and ready for use not later than the delivery period specified. If the supplier/Bidder fails to deliver any or all the stores or perform the service by the specified date, liquidated damages @0.5% per week or part thereof in respect of the value of the delayed stores will be deducted from the bill subject to a maximum of 10% value. Same terms are applicable for installation, training and demonstration clause mentioned above.

22. **Dispute and Jurisdiction:**

Any legal disputes arising out of any breach of contract pertaining to the whole process of this tender shall be settled in the court of competent jurisdiction in the district of Dharwad, Karnataka.

23. **Acknowledgement by the Bidder:**

It is hereby acknowledged that we have gone through all the schedules as well as the conditions mentioned above and we agree to abide by these.

Date:
Signature of the Bidder along with official seal.
Place:

CANVASSING OR OFFERING AN ADVANTAGE OR ANY OTHER INDUCEMENT BY ANY PERSON WITH A VIEW TO INFLUENCING ACCEPTANCE OF A BID WILL BE AN OFFENSE UNDER LAWS OF INDIA. SUCH ACTION WILL RESULT IN THE REJECTION OF BID, IN ADDITION TO OTHER PUNITIVE MEASURES.

Sd/-
Assistant Registrar (MMD), IIT Dharwad
(For and on behalf of Director, IIT Dharwad)

# Section II: Instructions to Bidders

1. Any bidder from a country which shares a land border with India will be eligible to bid in this tender only if the bidder is registered with the Competent Authority. (Refer to OM No. F.No.6/18/2019-PPD dt. 23/07/2020 of Ministry of Finance).

2. "Bidder" (including the term 'tenderer', 'consultant' or 'service provider' in certain contexts) means any person or firm or company, including any member of a consortium or joint venture (that is an association of several persons, or firms or companies), every artificial juridical person not falling in any of the descriptions of bidders stated hereinbefore, including any agency branch or office controlled by such person, participating in a procurement process.

3. "Bidder from a country which shares a land border with India" for the purpose of this Order means: -

   a. An entity incorporated, established or registered in such a country; or
   b. A subsidiary of an entity incorporated, established or registered in such a country; or
   c. An entity substantially controlled through entities incorporated, established or registered in such a country; or
   d. An entity whose beneficial owner is situated in such a country; or
   e. An Indian (or other) agent of such an entity; or
   f. A natural person who is a citizen of such a country; or
   g. A consortium or joint venture where any member of the consortium or joint venture falls under any of the above

4. The beneficial owner for the purpose of (iii) above will be as under:

   i. In case of a company or Limited Liability Partnership, the beneficial owner is the natural person(s), who, whether acting alone or together, or through one or more juridical person, has a controlling ownership interest or who exercises control through other means.

Explanation-

   a) "Controlling ownership interest" means ownership of or entitlement to more than twenty-five per cent. of shares or capital or profits of the company;
   b) "Control" shall include the right to appoint majority of the directors or to control the management or policy decisions including by virtue of their shareholding or management rights or share holders agreements or voting agreements;

   ii. In case of a partnership firm, the beneficial owner is the natural person(s) who, whether acting alone or together, or through one or more juridical person, has ownership of entitlement to more than fifteen percent of capital or profits of the partnership;

   iii. In case of an unincorporated association or body of individuals, the beneficial owner is the natural person(s), who, whether acting alone or together, or through one or more juridical person, has ownership of or entitlement to more than fifteen percent of the property or capital or profits of such association or body of individuals;

   iv. Where no natural person is identified under (1) or (2) or (3) above, the beneficial owner is the relevant natural person who holds the position of senior managing official;

   v. In case of a trust, the identification of beneficial owner(s) shall include identification of the author of the trust, the trustee, the beneficiaries with fifteen percent or more interest in the trust and any other natural person exercising ultimate effective control over the trust through a chain of control or ownership.

5. An Agent is a person employed to do any act for another, or to represent another in dealings with third person.

6. **Cost of Bidding**:
   The Bidder shall bear all costs associated with the preparation and submission of its Bid and the Purchaser shall not be held responsible or liable for those costs incurred regardless of the conduct or outcome of the bidding process.

7 **Amendments to Tender Document**:

i. At any time prior to the deadline for submission of bids, IIT Dharwad may, for any reason, whether on its own initiative or in response to the clarification sought by a prospective BIDDER may modify the bid document by issuing necessary corrigendum.

ii. All prospective BIDDERs who have downloaded the tender document are requested to visit IIT Dharwad website for any amendments / modifications and make a note of the same, which will be binding on them.

8 **Bid Opening Process**:

i. In case of one bid system, technical & financial bid will be opened simultaneously in the presence of representatives of the bidders at IIT Dharwad.

ii. In case of two bid system, The Technical Bid will be opened in the first instance in the presence of Technical Evaluation Committee (TEC)/MMD & representatives of the bidders at IIT Dharwad.

iii. Financial bids of only those bidders, whose bids are found technically qualified, by the Technical Evaluation Committee, will be opened in the presence of the Technical Evaluation Committee (TEC)/MMD & bidders' representatives subsequently at a later date for further evaluation. Date and Time of financial bid opening shall be intimated to technically qualified bidders only.

iv. One authorized representative of each of the bidder would be permitted to be present at the time of opening of the bids.

v. The authorized representative of bidders, present at the time of opening of the bids shall be required to sign an attendance register as a proof of having attended the Technical/Commercial bid opening session.

9 **Supplementary offer /Modification of Original Bid**:

BIDDER desirous to modify their offer/terms may submit their revised / supplementary offer (s) strictly within the Tender Opening Date (TOD) by clearly stating to the extent of updation done to the original offer. The purchaser reserves the right to open the original offer along with the revised offer.

10 **Confidentiality**:

i. Information relating to the evaluation of bids, and recommendation of Contract award, shall not be disclosed to Bidders or any other persons not officially concerned with such process until information on Contract award is communicated to all Bidders. On completion of Technical Evaluation by the Committee, Vendors whose offer do not meet with the users Technical Specification will be restricted to participate in commercial bid opening process. Information regarding the criteria for disqualification of the tender would be communicated to the bidder in writing (preferably through email provided in the bid).

ii. Any attempt by a Bidder to influence the Purchaser in the evaluation of the Bids or Contract award decisions may result in the rejection of its Bid.

iii. Notwithstanding, from the time of Bid opening to the time of Contract award, if any Bidder wishes to contact the Purchaser on any matter related to the bidding process, it must be done either through e-mail or in writing.

11 **Deviation, Reservations and Omissions**:

During the evaluation of Bids, the following definitions apply:

i. "Deviation" is a departure from the requirement specified in the Tender Documents;

ii. "Reservation" is the setting of limiting conditions or withholding from complete acceptance of the requirements specified in the Tender Documents; and

iii. "Omission" is the failure to submit part or all of the information or documentation required in the Tender Documents.

12 **Correction of Arithmetical Errors**:

i. Provided that the Bid is substantially responsive, the Purchaser shall correct arithmetical errors on the following basis:

i. if there is a discrepancy between the unit price and the line item total that is obtained by multiplying the unit price by the quantity, the unit price shall prevail and the line item total shall be corrected, unless in the opinion of the Purchaser there is an obvious misplacement of the decimal point in the unit price, in which case the line item total as quoted shall govern and the unit price shall be corrected;
ii. if there is an error in a total corresponding to the addition or subtraction of subtotals, the subtotals shall prevail and the total shall be corrected; and
iii. if there is a discrepancy between words and figures, the amount in words shall prevail, unless the amount expressed in words is related to an arithmetic error, in which case the amount in figures shall prevail subject to (a) and (b) above.

ii. Bidders shall be requested to accept correction of arithmetical errors. Failure to accept the correction in accordance with the same, shall result in the rejection of the Bid.

13 **Evaluation of Bid**:

i. Technical bids will be evaluated for suitability as per documentary validation, eligibility criteria and technical specifications laid out in this tender document. The bids found suitable will be recommended by the Procurement committee and after approval of competent authority shall be deemed as technically suitable offers. The technically qualified bidders will be informed accordingly and commercial bids of such offers will be evaluated on a suitable designated time and date. Unopened commercial bids of the other bidders, who are not found technically suitable will be returned.
ii. IIT Dharwad will evaluate technical and commercial acceptable offers on landed **Net Price basis**.
iii. In case any BIDDER is silent on any clauses mentioned in this tender documents, IIT Dharwad shall construe that the BIDDER had accepted the clauses as per the invitation to tender no further claim will be entertained.
iv. No revision in the terms and conditions quoted in the offer will be entertained after the last date and time fixed for receipt of tenders.

14 **Price Bid (For Indigenous Supplies to be quoted in INR only):**

i. Quoting of Price (s): **Price quoted should be in Indian Rupees only and free delivery at IIT Dharwad Campus site.**
ii. **PRICE BID must be submitted in enclosed Price Bid Format only (designed for indigenous/local supplies only).**
iii. Prices should include all the taxes including concessional GST @5% (as applicable) and all other duties/levies.
iv. If the price is not quoted in Price Bid Format provided in the tender document then, IIT Dharwad will reject the bid. The bidders are required to attach their blank price bid format in technical bid documents for this purpose (without indicating the price quoted).
v. If the bidder wishes to give pricing details, it may be attached in separate sheet. It is requested not to quote optional or multiple items, otherwise your quote may be rejected. The bidders are requested to quote only one option satisfying the tender terms & not multiple options.

15 **Corrupt & Fraudulent Practices**:

IIT Dharwad requires that bidders, suppliers, contractors and consultants, if any, observe the highest standard of ethics during the procurement and execution of such contracts. In pursuit of this policy, the terms set forth below are defined as follows:

i. "Corrupt practice "means the offering, giving, receiving, or soliciting, directly or indirectly, of anything of in kind/value to influence the action of a public official in the procurement process or in contract execution;
ii. "Fraudulent practice" means a misrepresentation or omission of facts in order to influence a procurement process or the execution of a contract;
iii. "Collusive practice" means a scheme or arrangement between two or more bidders, designed to establish bid prices at artificial, non- competitive levels; and

iv. "Coercive practice" means harming or threatening to harm, directly or indirectly, persons or their property to influence their participation in the procurement process or affect the execution of a contract;

IIT Dharwad will reject a proposal for award if it determines that the Bidder recommended for award has, directly or through an agent, engaged in corrupt, fraudulent, collusive or coercive practices in competing for the Contract in question.

16 **Cancellation of Tender**:

i. Notwithstanding anything specified in this tender document, IIT Dharwad in its sole discretion, unconditionally and without assigning any reasons, reserves the rights:
   1. To accept or reject lowest tender or any other tender or all the tenders.
   2. To accept any tender in full or in part.
   3. To reject the tender offer not conforming to the tender terms.
   4. To cancel the tender at any stage during the evaluation & before award of work

ii. Offer which deviates from the vital conditions (as illustrated below) of the tender shall be rejected:
   1. Non-submission of complete offers as mentioned in the tender document,
   2. Receipt of offers after due date and time and or by email / fax (unless specified otherwise).
   3. Receipt of offers in open condition.
   4. Conditional Tenders and Unsigned Tenders will also be rejected.

17 **Delivery**:

The successful BIDDER should deliver the material as per tender document/purchase order. **The successful bidder should also emboss stickers of purchase order number on the material to be delivered at IIT Dharwad.**

Sd/-
Assistant Registrar (MMD), IIT Dharwad
(For and on behalf of Director, IIT Dharwad)

# Section III: Conditions of Contract

1. Award of Contract:
   a) **IIT Dharwad shall award the contract to the technically qualified eligible BIDDER whose bid has been determined as the lowest evaluated commercial bid under this tender subject.**
   b) If more than one BIDDER happens to quote the same lowest price, IIT Dharwad reserves the right to award the contract to more than one BIDDER or any BIDDER.

2. **Prices & Taxes applicable (Customs Duty / IGST / SGST / CGST):**
   a) **For Indigenous Supplies (bids in INR) - As per Govt. of India Notification No. 47/2017-Integrated Tax (Rate) dt. 14th November 2017, Notification No. 45/2017-Central Tax (Rate) dt. 14th November 2017 and Notification No. 45/2017-Union Territory Tax (Rate) dt. 14th November 2017; IIT Dharwad is eligible to avail concessional GST rates. The applicable rate of IGST shall be 5% in case of Inter-state purchase and shall be the same as 5% (CGST @2.5% & SGST @2.5%) in case of purchases within the state.** We shall provide the concessional GST certificate under this notification to enable you to deliver the goods as per the rates specified and to raise an invoice subsequently on this rate only. The supplier shall pay and bear all other liabilities, taxes and duties not specifically agreed by the Purchaser in the contract.

3. Pre-installation:
   Please also mention the pre-installation requirements for the equipment like ambient temperature, humidity, civil work, weather specifications, power specifications, etc. When all items are provided, full performance satisfaction should be demonstrated to IIT Dharwad.

4. Installation:
   a) BIDDER shall be responsible for installation wherever applicable and for after sales service during the warranty period and thereafter as mentioned in the contract.
   b) Installation, demonstration and training to be arranged by the supplier within the quoted price and the same is to be done within 15 days of the arrival of the equipment at site or whenever informed by IIT Dharwad.

5. **Terms of Payment (For Indigenous Supplies and quotes in INR):**
   i. Payment within 30 days from the date of successful delivery, installation and receipt of Acceptance Certificate of concerned Department / Section / Materials Management Division, IIT Dharwad.
   ii. Payment shall be made by electronic fund transfer or such other mode offered by the Bank.
   iii. IIT Dharwad does not pay advance payment to party. Any request of Advance payment will be summarily rejected.

6. Transfer and Subletting:
   The seller shall not sublet, transfer, assign or otherwise part with the acceptance to the tender or any part thereof, either directly or indirectly, without the prior written permission of the Purchaser.

7. Force Majeure:
   Force Majeure will be accepted on adequate proof thereof.

8. Specification and Samples:
   The suppliers shall supply the stores in accordance with the specifications/ descriptions of stores given in the acceptance of tender. The Purchaser reserves the rights to alter the description of stores including drawings given in the acceptance of tender. In the event any such alteration result in any implication to the delivery and price, such implication shall be mutually agreed between the Purchaser and supplier.

9. Supervision of Erection and Commissioning:

Successful BIDDER shall depute concerned specialist, for supervision of erection & commissioning of the machine to be carried out. The successful BIDDER shall make necessary arrangement at their own expenses for stay, transport and other expenses of their specialist during their stay in Dharwad which also includes imparting free of cost training to IIT Dharwad personnel.

10. **Performance Guarantee (GFR 2017 Rule 171):**

i. Performance Guarantee Bond is mandatory.

ii. Successful tenderer/ bidder should submit performance guarantee on or before 15 days from the date of issue of order acknowledgement. The PBG to be furnished in the form of bank guarantee as per proforma, for an amount covering 3% of the purchase order value.

iii. The Performance Guarantee should be established in favour of "The Registrar, IIT Dharwad".

iv. PBG to be established through any of the National Banks/Scheduled bank (whether situated at Dharwad or outstation) with a clause to enforce the same on their local branch or any scheduled bank (other than National bank). Bonds issued by co-operative banks will not be accepted.

v. Performance Guarantee Bond shall be for the due and faithful performance of the contract and shall remain binding, notwithstanding such variations, alterations for extensions of time as may be made, given, conceded or agreed to between the successful tenderer and the purchaser under the terms & conditions of acceptance to the tender.

vi. The successful tenderer is entirely responsible for due performance of the contract in letter and spirit and all other documents referred to in the acceptance of tenders.

vii. The PBG shall be kept valid during the period of contract and shall continue to be enforceable for a period (as mentioned in the tender document) or up to warranty period whichever is later from the date of order acknowledge. In case PBG needs extensions up to warranty period then supplier shall initiate extensions to PBG one month prior to expiry of PBG. For successful suppliers, if PBG is not submitted within **15 days** from the date of Order Acknowledgement, then the Purchase Order may be cancelled.

viii. **No interest shall be payable by the buyer to the Bidder on PBG.**

## FORMAT FOR BID SECURITY DECLARATION

(To be typed on Firms letterhead)

I/We will not withdraw or modify the bid submitted by me/us during the period of validity or if awarded the contract and fail to sign the contract or to submit a performance security before the deadline defined in the tender document.

Yours sincerely,

Date: **(Authorised signature & seal of the bidder)**

Address:

## FORMAT FOR PERFORMANCE GUARANTEE BOND

(To be typed on Non-judicial stamp paper of the value of One Hundred Indian National Rupees)

{TO BE ESTABLISHED THROUGH ANY OF THE NATIONALIZED BANKS/SCHEDULED BANKS WITH A CLAUSE TO ENFORCE THE SAME ON THEIR LOCAL BRANCH OR ANY SCHEDULED BANK (OTHER THAN NATIONALIZED BANK). BONDS ISSUED BY CO-OPERATIVE BANKS ARE NOT ACCEPTED}

To,
The Assistant Registrar (MMD)
Indian Institute of Technology Dharwad
WALMI Campus, Dharwad – 580011

***LETTER OF GUARANTEE***

WHEREAS Indian Institute of Technology Dharwad (Buyer) have invited Tenders vide Tender No..... Dt. ..... for purchase of ..... AND WHEREAS the said tender document requires that any eligible successful tenderer (seller) wishing to supply the equipment / machinery, etc. in response thereto shall establish an irrevocable Performance Guarantee Bond in favour of **"The Registrar, Indian Institute of Technology Dharwad"** in the form of Bank Guarantee for Rs. ..... **{@3% (three percent) of the purchase value}** and valid till **one year or up to OEM warranty period whichever is later** from the date of issue of Performance Guarantee Bond is required be submitted within 15 (Fifteen) days from the date of Order Acknowledgment as a successful bidder.

NOW THIS BANK HEREBY GUARANTEES that in the event of the said tenderer (seller) failing to abide by any of the conditions referred in tender document / purchase order / performance of the equipment / machinery, etc. this Bank shall pay to Indian Institute of Technology Dharwad on demand and without protest or demur Rs ..... (Rupees.....).

This Bank further agrees that the decision of Indian Institute of Technology Dharwad (Buyer) as to whether the said Tenderer (Seller) has committed a breach of any of the conditions referred in tender document / purchase order shall be final and binding.

We, ..... (name of the Bank & branch) hereby further agree that the Guarantee herein contained shall not be affected by any change in the constitution of the Tenderer (Seller) and/ or Indian Institute of Technology Dharwad (Buyer).

**Notwithstanding anything contained herein:**

iii. Our liability under this Bank Guarantee shall not exceed Rs. .....(Indian Rupees ..... only).
iv. This Bank Guarantee shall be valid up to .....(date) and
v. We are liable to pay the guaranteed amount or any part thereof under this bank guarantee only and only if IIT Dharwad serve upon us a written claim or demand on or before .....(date).

This Bank further agrees that the claims if any, against this Bank Guarantee shall be enforceable at our branch office at ..... situated at ..... (Address of local branch).

Yours sincerely,

Date:

Signature and seal of the guarantor:
Name of Bank:

Address:

**Instruction to Bank: Bank should note that on expiry of Bond Period, the Original Bond will not be returned to the Bank. Bank is requested to take appropriate necessary action on or after expiry of bond period.**

# Section IV – Complete Schedule of Requirements and Compliance

| This section has following compliance requirements: | |
|---|---|
| i | Compliance for commercial terms and conditions of tender |
| ii | Compliance for technical specifications of the equipment to be supplied |
| iii | Bidders information & Reasonability of prices |

## i. Table of compliance for commercial terms & conditions of tender (to be filled by bidder)

**(NO FIELD TO BE LEFT BLANK)**

| S. No. | Terms and Conditions | IIT Dharwad tender requirements | Response by Bidder M/s _____ |
|---|---|---|---|
| 1 | Nature of supply (to be specified) | Indigenous/Local supply | |
| 2 | Price Bid Currency (to be specified) | Local then INR only | |
| 3 | Delivery terms (to be specified) | Indigenous/Local then Door Delivery (Refer point 17 of Section-I) | |
| 4 | Freight & Insurance | Confirm point 18 of Section-I | |
| 5 | Warranty for three years from the date of installation and Commissioning. Offer for 3 years AMC after the completion of warranty period clearly indicating the scope of AMC | Confirm point 19 of Section-I | |
| 6 | Supply & Installation | Confirm point 20 of Section-I | |
| 7 | GST Rate (If Local supply in India) | Applicable rate @ 18% Confirm point 2 of Section-III | |
| 8 | Training & Pre-installation checks | Confirm point 3 of Section-III | |
| 9 | Terms of Payment | Confirm point 5 of Section-III | |
| 10 | PBG | Confirm point 10 of Section-III | |
| 11 | Complete tender document copy | Signed & stamped copy required | |
| 12 | PAN | Copy of PAN required | |
| 13 | GST | Copy of GST certificate required | |
| 14 | ITRs (2018-19 to 2020-21) | Last 3 financial years ITR required | |
| 15 | Proof of Business existence | For a period of more than 3 years required | |
| 16 | Previous Experience (Refer point 12 of Section-I) | At-least one performance certificate with Purchase Order copy is required | |
| 17 | Blacklisting status | Declaration required to confirm the status | |
| 18 | OEM Details | Please attach the OEM details | |
| 19 | Bidders Information | Please complete the table in point (iii) under Section-IV to ascertain all relevant details | |
| 20 | Reasonability of prices | | |

## ii. Table of compliance for technical specifications of the equipment to be supplied (REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES)

**SPECIFICATION OF 'SUPPLY, INSTALLATION, TESTING AND COMMISSIONING OF 'REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES'** AS PER BELOW GIVEN TECHNICAL SPECIFICATIONS AND FEATURES

**TECHNICAL DATA:**
Technical Particulars to be filled in by vendor with documentary evidence

**General Specification**

The requirement is for the use of state-of-the-art Real Time Hardware in the Loop Simulation System (HILS System) for testing and integrating various electrical systems such as integrated renewable energy, Energy Storage, DER's, power electronics and drives, and other smart grid systems, using functional dynamic models with the actual hardware in order to develop and study solutions suitable for the next generation electrical systems.

The institute intends to procure a HILS system which will be integrated with various controllers and electrical systems.
Recognizing that the HIL simulator is needed for the long-term, with multiple projects and programme objectives, supplier should provide modular hardware architecture:

- Scalable Processing – multi-core/multi-processor/multi-FPGA architecture to meet real-time model computation requirements. A basic configuration can be used for simple models and expanded as computational needs increase with the use of more complex models for higher simulation fidelity.

- Expandable I/O and Signal Conditioning– the I/O chassis should support multiple I/O modules as well as third-party boards. Supplier should be able to provide several modules of I/Os, any Change or increase in I/O requirements should be accommodated by replacing/adding modules and cards at any point of time. Since projects will be running for multiple years, scope of adding or removing the I/O module should be available.

- Commercial RTOS used should support wide range of software tools to run in real time environment. This capability will be critical for our projects which will be using the in house developed Simulink Models, Certified C Code, FORTRAN and third party tools like PSS/E, Plexim etc. It should also support CYME or Digisilient software packages if required in future.

- Test automation should support tools like Python, LabView TestStand, Altia, PROVETech etc. This will help IITDH to achieve complete testing of hardware for the various conditions.

- Vendor should supply an OPEN but fully integrated solution, HIL system should have high degree of FLEXIBILITY to meet a variety of testing objectives.

## III. Detailed specifications

Detailed requirement of the real time simulator system are given below:

**HiLS System Level**
The system-level requirements that are to be satisfied by the HiLS System are given below:

- Systems offered should be primarily designed for hard real-time high fidelity simulation of electrical systems. The purpose is to aid in the design and development of prototypes of controllers and monitoring systems, suitable for implementation in actual electrical systems.

- Industry production standard hardware platforms based on PC technologies (with multi-core, multi-processor motherboards, PCIe/VME/PXI and Gigabit Ethernet communication capabilities) with emphasis on open architecture for ensuring interoperability with products of industry-leading manufacturers of similar systems.

- Multi-node or multi-core distributed architecture with I/O capabilities with direct linkage to I/O modules or systems to ensure reduction of model-I/O communication overheads and latencies in closed loop operation.

- Real-time communication through external communication links amid all the nodes for deterministic exchange of parameters amongst models or through shared memory in case of execution of models in multi-core system with appropriate clock synchronization through master slave mechanism.

- Software framework for assignment of models to various nodes/cores/subunits and distribution of executable software models to respective nodes/cores/subunits for simultaneous execution and control of specific I/O, in hard real-time, using an RTOS, in frame-synchronised manner, at simulation time steps as fast as 20 us, to achieve high fidelity with respect to the performance of the actual systems.

- Real time computation of complete electro-mechanical systems up to an assured time-step of 20 microseconds. Multi-rate simulation should be possible. With FPGA based simulation for Power Electronics simulation time step should be as low as 150ns. It should be able to simulate power electronic circuits having up to 72 switches and step time of 5 micro seconds.

- Re-configurable FPGA based simulation, debugging and execution capabilities, with direct control of I/O interfaces to external hardware.

- Test script generation, execution and intrusive/non-intrusive debugging in manual, interactive mode as well as in automatic mode.

- User friendly GUI for selecting signals and parameters for display and plotting at run-time

- Test results display as well as recording/logging in on-line mode in on-board hard disk storage

**Specification details for HIL Platform**

| Items | Details | Specifications | Whether complied Yes or no | Specifications of the quoted product |
|---|---|---|---|---|
| **HIL Hardware with accessories** | General Features of Hardware | • Simulator with a capability to simulate a minimum of 50 3-ph bus system at 20-50 micro-seconds with provision for expandability<br>• Simulator with a capability to perform closed loop testing of protection relays with a provision to interface with existing amplifiers if need be.<br>• Simulator with a capability to simulate control logic required for renewable energy, power systems, power electronics and drives applications.<br>• Hardware architecture should be modular in nature to allow future expansion.<br>• Ethernet communication and control ability via standard LAN infrastructure to one or many standard computer workstations.<br>• The computational unit shall preferably consist of primarily off the shelf computer technology.<br>• FPGA based I/O cards to minimize latency in ADC, DAC, DI, and DO.<br>• Minimum count of I/O must be 16 Analog i/p, 16 Analog o/p, 32 digital i/p & 32 digital o/p.<br>• A user programmable FPGA must be available to do fast power electronics simulations.<br>• Rack mountable chassis for scalability.<br>• Supplied hardware should to support communication protocol for smart grid applications like C37.118, etc./IEC61850, DNP3,Modbus should be supported if required for future application | | |
| | **Simulator Chassis** | Simulator Chassis should be rack mountable it should have minimum specifications given below | | |
| | | a. Powerful target computer, with Multi Core Processor, Minimum Quad core | | |
| | | b. Minimum supported speed 3.5Ghz | | |
| | | c. Supported SDD, Minimum 256GB | | |
| | | d. Supported DDR RAM, minimum 16GB | | |
| | | e. Should have PCIe slots to support third party cards/custom made cards | | |

| Items | Details | Specifications | Whether complied Yes or no | Specifications of the quoted product |
|---|---|---|---|---|
| | | f. Should have SFP Ports- Minimum 8 Ports SFP communication and Optical cable should be provided to interface with multiple units to run one large simulation | | |
| | **Analog Inputs-16 Ch** | ADC should ensure simultaneous signal capture from multiple channels, and should eliminate skew errors associated with multiplexed channels. Specification are given below | | |
| | | a. Minimum 16 differential channels with independent 16 bit ADCs, 2.5 us conversion time, simultaneous conversion, controlled by on-board FPGA | | |
| | | b. Capability to convert analog signal between the base simulator time steps to implement special models and signal processing functions with time step of 2.5 us depending on A/D converter speed selected | | |
| | | c. Gain and offset calibration factor adjustable by software | | |
| | | d. The same card should be capable of reading 6 resolver signals from the device/controller. | | |
| | | e. Analog i/p voltage Range: ± 20V | | |
| | **Analog Outputs-16 Channels** | DAC should ensure simultaneous signal generations for multiple channels and should eliminate skew errors associated with multiplexed channels. Specification are given below: | | |
| | | a. 16 channels of independent 16-bit DACs, 1.0 us settling time/channel, simultaneous conversion on all channels controlled by on-board FPGA | | |
| | | b. Buffered Output Stage with Voltage range of ± 15V or higher | | |
| | | c. Capability to control the conversion time of each channel by the FPGA | | |
| | | d. Capability to convert analog signal between the base simulator time step to implement special models and signal processing functions with time step of 1 us | | |
| | | e. Gain and offset calibration factor adjustable by software | | |
| | | f. Short-circuit protection. | | |
| | **Digital Inputs-32 Channels** | Digital input module should be versatile and provide digital inputs with specific voltage conditioning. It should support for the voltage isolation. All channels should be sampled simultaneously for better accuracy. It should take real life TTL or differential level signals. Specification are given below | | |

| Items | Details | Specifications | Whether complied Yes or no | Specifications of the quoted product |
|---|---|---|---|---|
| | | a. 32 independent channels. | | |
| | | | | |
| | | b. Current input from 2 mA to 6 mA | | |
| | | c. Input current protection by a resettable solid-sate fuse | | |
| | | d. Input voltage adjustable from 5 V to 30V | | |
| | | e. Optical-isolation on all channels is a must | | |
| | | f. Short-circuit protection at 100 mA | | |
| | | g. Software configurable PWM input on the same card for a frequency of 100 Khz (minimum)<br>Should support reading atleast 16 PWM signals simultaneously | | |
| | **Digital Output-32 Channels** | Digital Output module should be versatile and provide digital output signal with specific voltage conditioning. It should support for the voltage isolation. All output channels should be sampled simultaneously for better accuracy. It should interface with real life TTL or differential level signals. Specifications are given below | | |
| | | a. 32 independent push-pull channels per module/card | | |
| | | b. O/P Voltage (configurable) upto 20V<br>O/P Current 30mA Sink or Source | | |
| | | c. All outputs are generated simultaneously with a maximum transition delay of 50ns | | |
| | | d. Short-circuit protected output | | |
| | | e. Software configurable PWM output on the same card for a frequency of 100 Khz (minimum) | | |
| **Power Amplifier** | **General Specification** | Switching Frequency > 1kHz | | |
| | | Ambient Temperature : 10-45°C | | |
| | | Humidity : 95% RH or less (no condensation) | | |
| | | Test points : 3 voltages & currents on i/p side and 3 voltages & currents on o/p side | | |
| | **Input Specification** | Supply Voltage : 3-phase, 415V, 50Hz | | |
| | | Input Voltage Tolerance : +10% | | |
| | | Input Frequency : 50Hz | | |
| | | Input Frequency Tolerance : ±2% | | |
| | | I/P Power Factor : 0.9 or higher at Rated conditions | | |
| | **Output Specifications** | Output Voltage : 3-phase ,4 wire, Isolated 415V | | |

| Items | Details | Specifications | Whether complied Yes or no | Specifications of the quoted product |
|---|---|---|---|---|
| | | Output Apparent Power : 11.25 kVA | | |
| | | Output power : 9 kW | | |
| | | Output Frequency : 50HZ ,± 2Hz | | |
| | **Protections** | Input Under voltage | | |
| | | Input Over voltage | | |
| | | Input over current | | |
| | | Input short circuit | | |
| | | Output under voltage | | |
| | | Output over voltage | | |
| | | Output over current | | |
| | | Output short circuit | | |
| | | Over temperature | | |
| **HIL Software** | | | | |
| | **Modeling Environment** | • Modelling environment should be capable of simulating models created with MATLAB/ Simulink/ Simscape/ SimPoweSystems/ Plecs.<br>• IITDH intends to use these offline simulation softwares which are available in IITDH<br>• Should aid development of custom logic & algorithms used in advanced control schemes ( e.g., C s-function).<br>• The Integrated Development Environment Host software should allow users to run simulations on a windows target in non-real time mode, for testing/validation without real-time simulation.<br>• Software should be capable of generating PWM pulses independent of simulation clock.<br>• FPGA programming environment interface, which can be used for faster converter simulation, must be available<br>• Provision to perform load flow studies.<br>• Ability to edit parameters of the system during real time execution.<br>• Automatic Core Allocation in cases of Multi-core simulation which will help us in minimizing time and effort to allocate cores manually should be available. It should also allow manually assigning core.<br>• Should have the capability for FPGA-based simulation environment of power electronics systems using model built using Graphical Circuit Editors like | | |

| Items | Details | Specifications | Whether complied Yes or no | Specifications of the quoted product |
|---|---|---|---|---|
| | | Simscape, PLECS, PSIM, PSPICE eliminating direct programming of the FPGA using VHDL. Provision of programming the FPGA should be available if needed in future.<br>• Editable example models for teaching in the field of Drives and Power Electronics etc must be provided compatible to SimPowerSystems or Simscape to get started quickly for students.<br>• Features to simulate micro-grids with distributed energy resources such as wind, solar PV etc. with example models of PV Inverters, wind generators etc.<br>• Provision to simulate the distribution system.<br>• Feature to display the time variations of any signal of interest.<br>• Capability of a minimum multiple drives and detailed inverter models at a time step of 25 microseconds on CPU and 150ns on FPGA.<br>• Ability to simulate PMSM drives in 250 ns (end-to-end) (useful feature for drives applications).<br>• Should have specialized solvers for Drives and Power electronic systems<br>• Should have provision for scripting language (e.g. Python).<br>• Ability for other third party Simulations software like GT-Power, AMESim, TESIS, etc.<br>• Modelling environment for Power Electronics, Drives and Control Systems is preferred to be compatible with MATLAB environment due to extensive usage of the same at IIT Dharwad<br>• Ability to take care of multiple events happening in between time steps.<br>• Ability to perform real time simulation of power electronics converters up to a switching frequency of 100 kHz.<br>• Ability to simulate at least 3-level converter with a switching frequency of 100 kHz.<br>• Simulation of minimum 30-40 average converter models (Three phase) with detailed control loops and simulation time-step of 500ns or less<br>• Simulation of minimum three or more switching converter models (Three | | |

| Items | Details | Specifications | Whether complied Yes or no | Specifications of the quoted product |
|---|---|---|---|---|
| | | phase) with simulation time-step of 500 ns. | | |
| | | Interfaces should be GUI based as much as possible to make it easy to configure, and edit the parameter on the fly | | |
| | | Model-based FPGA programming environment interface to enable simulation of high fidelity models of power converters | | |
| | | Software environment ability to create automated test scripts in languages such as Python | | |
| | **Phasor Simulation** | Simulating electro-mechanical transient stability phenomenon of very large power grids with thousands of buses, generators, transformers, transmission lines, loads and controllers. Should use a fundamental frequency solver optimized to compute rms values of voltages, currents, active and reactive power in real time, with a typical time step of 1 milliseconds. | | |
| | | Should simulate power grid with 1000, 3Ø Buses in Real Time | | |
| | | Should be able to build the circuit using the standard C++ library (machines, loads, transformer etc..) | | |
| | | Should be able to build circuit using the FMI library (with standard exciters, PSS, machines etc..) | | |
| | | Should possible to import user defined components developed with modelica software through FMU | | |
| | | Should support simulation of models built in PSS/E. | | |
| | **Communicatio n Protocol** | C37.118 drivers for fast transmission and reception of synchro phasor streams, according to the IEEE C37.118 standard, typically composed of a set of 3 voltages and 3 currents (magnitudes and angles). | | |
| | | Synchronization through GPS, IEEE 1588, IRIG-B or 1PPS | | |
| | | Should support up to 240 frames per second | | |
| | | Number of PMUs to be simulated-100 Nos across the power system network | | |
| | | Support class M and P equipment | | |

| Items | Details | Specifications | Whether complied Yes or no | Specifications of the quoted product |
|---|---|---|---|---|
| | | Interface PMU, PDC, Scada, control and protection equipment | | |
| | | Compatible with C37.238-2011 standard for precision time stamping | | |
| | Time Sync Adaptor | | | |
| | Standards | IEEE 802.3-2000<br>IEEE 1588-2008 | | |
| | Supported functions | IEEE 1588 hardware timestamping<br>IEEE 1588 hardware clock 4 programmable IO ports GPS receiver | | |
| | Operation | PTP master and slave | | |
| | High Precision hardware time stamping | Should be possible | | |
| | | Single vendor should supply the complete hardware and software as per the given specification. | | |
| | | Vendor should provide onsite training, and familiarize IITDH officials for operation of the test facility. | | |
| | | Vendor provided solution must be based on COTS hardware. It must be scalable and flexible allowing easy integration with new controllers or new hardware. | | |
| | | Vendor should demonstrate all features to the user as part of TEC (Technical evaluation Committee). | | |
| | | IITDH has developed Simulink/PSSe models for electrical systems. These models should be ported on to the test facility. | | |
| | | Software warranty five years from the date of successful installation at IIT Dharwad. | | |

**Required Application for Power system and Power Electronics.**

1) Execute MATLAB Simulink/SimPowerSystems or Simscape models directly in real time
2) Perform both plant and/or controller simulation using the same platform for Hardware In Loop (HIL) and Rapid Control Prototyping (RCP) applications
3) Execute transmission network like IEEE large bus benchmark systems with detailed model of generators, controls, transformers, transmission lines and loads
4) Simulate detailed IEEE distribution systems up to IEEE 13 bus system
5) Simulate detailed Wind power plant using DFIG or PMSG
6) Execute detailed model of multiple solar PV panels based PV farm

7) Simulate CIGRE benchmark two-terminal LCC-HVDC
8) Simulate various FACTS devices like SVC, TCSC, STATCOM, UPFC
9) Simulate power converters associated with RE sources operating at switching frequency up to 2 kHz
10) Send up to 16 CT/PT/CVT signals to actual protection relays, PMUs and other Intelligent Electronic Devices (IEDs)
11) Receive up to 32 status/command signals in the form of digital inputs from external controllers and components
12) Perform closed loop testing of low voltage interface protection relays for different contingencies in the power network
13) Detailed simulation of 2-level, 3-level converters used in medium voltage industrial drives applications with switching frequencies as high as 2 kHz.
14) Prototype control algorithms for laboratory scale converters used in renewable energy, power quality applications etc.
15) Test in closed loop 2-level and 3-level inverters for drives and power conversion applications
16) Prototype control of wind energy systems using DFIG or PMSG
17) Control a wind turbine emulator system using DC motor setup
18) Prototype different control schemes associated with Solar PV inverters
19) Validate control algorithms of Switched Mode Power Supply (SMPS) and UPS
20) Test industrial controls for drives such as Direct Torque Control, V/f etc.
21) I/O channels: 16 Analog output, 16 Analog input, 32 Digital input, 32 Digital output
22) Simulation of power converters of up to 64 switches at a time step as low as 250 ns. Thus, having a high fidelity power electronic real-time simulation. The user can therefore, easily have converter switching frequencies as high as 50 kHz.
23) Should be possible to simulate different types of converter topologies & should be possible to simulate on FPGA without requiring direct FPGA programming.

Scalability

1. Supplied system should be scalable for the future requirement. It should be possible to add IO's later
2. Supplied systems should support required communication protocol which are used in drives application
3. Should be able to add software license at later point of time to increase the computation power
4. System supplied should be with COTS technology .

We, M/s _____ comply with the above requirements.

**(Authorised signature & seal of the bidder)**

**iii.**

Table for bidder information & reasonability of prices (to be filled by bidder)

## Bidders Information

| | | |
|---|---|---|
| 1. | Name of the Bidder | |
| 2. | Address of the Bidder | |
| 3. | PAN No. | |
| 4. | GST No. | |
| 5. | State of GST Registration | |
| 6. | E-mail<br>(for the purpose of official communication) | |
| 7. | Contact Person's Name & Designation | |
| 8. | Mobile No. | |
| 9. | Bank Details of the Bidder:<br>a. Name of the A/c Holder<br>b. Name of the Bank<br>c. Branch name<br>d. Account No.<br>e. IFSC Code<br>f. Any other detail | |

**(Authorised signature & seal of the bidder)**

## Reasonability of Prices

(Please quote best minimum prices applicable for premier Educational and Research Institution of National Importance)

## Previous Supply Orders

Name of the Firm _____

| Order placed by (Full address of Purchaser) | Order No. and Date | Quantity | Value of Order | Date of completion of delivery as per contract | Remarks indicating reasons for late delivery, if any and justification for price difference of their supply order & that quoted for IIT Dharwad | Has the Equipment been installed satisfactorily (Attach a Certificate from the Purchaser/ Consigner) | Contact Person along with Telephone No., Fax No. and e-mail address. |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

(Authorised signature & seal of the bidder)

# Section V Section - PRICE BID

## Indigenous / Local Supplies (to be quoted only in INR)

| Sl. No. | Short Description of Item (as per specifications mentioned in Section IV (ii) of tender document) | Qty. | HSN Code / SAC Code | Amount Quoted* (in INR only) |
|---|---|---|---|---|
| 1. | Supply & Installation of REAL-TIME SIMULATION AND HARDWARE-IN-LOOP PLATFORM WITH CPU AND FPGA BASED SIMULATION, MATLAB/SIMULINK MODEL COMPATIBILITY, AND ASSOCIATED SOFTWARE/LICENSES with five year warranty | 01 Nos. | | |
| 2. | IGST / CGST / SGST | | | |
| 3. | **GRAND TOTAL BID PRICE** | | | |

*** Please refer clause 7 & 17 (Section-I), clause 14 (Section-II) & clause 2 (Section-III) before quoting the prices.**
*** In case the bidder intends to provide the break-up of prices quoted, then a separate sheet to be attached.**
*** Price quoted should be inclusive of transportation, packing & delivery, installation, repair or replacement (if any)**

**(Authorised signature & seal of the bidder)**

Note-1: Price Bid should be submitted in given format only.
Note-2: The quantities mentioned above are subject to upward and downward revision, depending on the requirement of IIT Dharwad in future.